ATTORNEY DOCKET NO. BECKER 1 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Johannes Becker
Serial No.:	10/706,365
Filed:	November 12, 2003
Title:	SYSTEM AND METHOD FOR SECURING AN INTEGRATED CIRCUIT AS AGAINST SUBSEQUENT REPROGRAMMING
Grp./A.U.:	2435
Examiner:	Suman Debnath
Confirmation No.:	6816

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being electronically filed with United States Patent and Trademark Office on:
September 8, 2010 (Date)
Jana R. Williford
(Printed or typed name of person signing the certificate)
/Jana R. Williford/
(Signature of the person signing the certificate)

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

The Appellant has carefully considered this application in connection with the Final Examiner's Action electronically delivered July 8, 2010 (hereinafter "Office Action"), and respectfully requests a pre-appeal brief review of this application in view of the following remarks.

REMARKS/ARGUMENTS

Claims 1-4, 6-11, 13-18 and 20 are currently pending in the application.

I. Rejection of Claims 1-4, 6, 8-11, 13, and 15-18 under 35 U.S.C. §103

The Examiner has rejected Claims 1-4, 6, 8-11, 13, and 15-18 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,631,912 to Mote (hereinafter "Mote") further in view of U.S. Patent No. 7,124,340 to Bos, *et al.* (hereinafter "Bos"). The Appellant respectfully disagrees.

At item 19 at the top of page 6 of the Office Action, the Examiner states:

> Examiner maintains that Mote discloses port access circuitry on a integrated circuit (IC) that denies access to a memory of the IC when a testing port is disabled ("[t]he output enable bit held in the latch 217 can be used to enable or disable the entire memory bus interface 148 when in JTAG test mode" –e.g. see, col. 4, lines 31-62, see also FIG. 1; wherein IC 128 controls the access to memory system 140 through interface 148; access to memory 140 can either me (*sic*) disabled or enabled when in JTAG testing mode).

As the Examiner recognizes, Mote teaches enabling or disabling (when in JTAG mode) the entire memory bus interface 148. When latch 217 is used to disable the memory bus interface 148, access to memory 140 by first memory chip 110 is prohibited. However, even if access to memory 140 is prohibited by chip 110, this does not mean that all access to memory on chip 110 is denied. On the contrary, since Mote teaches that even if latch 217 disables access to memory bus interface 148, access to μP interface 138 and PCI interface 128 can still be enabled. Thus, access to memory on chip 110 is NOT denied but, rather, access to memory on chip 110 can be allowed through either μP interface 138 and/or PCI interface 128 since they can be enabled. Indeed, many operations by μP bus 135 and PCI bus 125 will access memory on chip 110 even if access to memory bus 145 is denied by disabling memory bus interface 148.

As such, while the cited portions of Mote may teach denying access to memory off of chip 110, the cited portions of Mote do NOT teach or suggest denying access to memory on chip 110 as recited in pending independent Claims 1, 8, and 15. Bos has not been cited to cure the above-noted deficiencies of Mote but to teach a testing port comprises a direct loopback between input and output pins thereof. Thus, the cited portions of the cited combination of Mote and Bos, as applied by the Examiner, does not provide a *prima facie* case of obviousness for pending independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Appellant respectfully requests the Review Panel to remove the §103(a) rejection of Claims 1-4, 6, 8-11, 13, and 15-18 and allow issuance thereof.

II. Rejection of Claims 7, 14, and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 7, 14 and 20 under 35 U.S.C. §103(a) as being unpatentable over Mote and further in view of Bos and U.S. Patent No. 6,522,100 to Hansford (hereinafter "Hansford"). As established above, the cited portions of the cited combination of Mote and Bos, as applied by the Examiner, do not provide a *prima facie* case of obviousness of pending independent Claims 1, 8, and 15. Hansford has not been cited to cure the above-noted deficiencies of the cited combination but to teach wherein the IC is a baseband chip of a mobile communication device. As such, the cited portions of the cited combination of Mote, Bos, and Hansford, as applied by the Examiner, do not establish a *prima facie* case of obviousness of pending independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Appellant respectfully requests the Review Panel to withdraw the §103(a) rejection of Claims 7, 14, and 20 and allow issuance thereof.

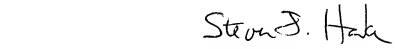
III. Conclusion

In view of the foregoing remarks, the Appellant respectfully submits that all of the Claims currently pending in this application are in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-4, 6-11, 13-18, and 20.

The Appellant requests the Reviewers to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
BECKER 1

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Application Number	Filed
10/076,365	November 12, 2003
First Named Inventor	
Johannes Becker	
Art Unit	**Examiner**
2435	Suman Debnath

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 58,076
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34

/Steven J. Hanke
Signature

Steven J. Hanke
Typed or printed name

972-480-8800
Telephone number

September 8, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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